In the Claims

Applicant has submitted a new complete claim set. Please cancel claims 18-25 without prejudice or disclaimer.

1. (original) An CMOS integrated circuit including analog and digital circuitry, said circuit having only two polysilicon layers on a CMOS substrate, wherein said digital circuitry includes an EEPROM memory comprising a floating gate formed from one polysilicon layer and a control gate formed from the other polysilicon layer, and said analog circuit includes at least one capacitor having one polysilicon electrode and one metal electrode.

2. (original) The integrated circuit of claim 1, wherein the analog circuitry comprises at least one analog-to-digital converter, and said at least one capacitor forms a component within said analog-to-digital converter.

3. (original) The integrated circuit of claim 2, wherein the analog-to-digital converter further includes a binary trim array for trimming out the capacitance variations resulting from the use of polysilicon - metal capacitors.

4. (original) The integrated circuit of claim 3, wherein said analog-to-digital converter is arranged to acquire calibration values for the trim array from said EEPROM.

5. (original) The integrated circuit of claim 4, wherein the analog-to-digital converter is arranged to acquire its calibration values at power up of the integrated circuit.

6. (original) The integrated circuit of claim 4, further including a micro-controller arranged to cause the analog-to-digital converter to acquire the calibration values.

7. (original) The integrated circuit of claim 3, further including a micro-controller arranged to write calibration values for said trim array to the EEPROM.

8. (original) The integrated circuit of claim 2, wherein said analog-to-digital converter has a plurality of channels, and calibration coefficients are associated with each one of the channels.

9. (original) The integrated circuit of claim 1, further including means for erasing said EEPROM by tunneling between said two polysilicon layers.

10. (original) The integrated circuit of claim 1, wherein the analog circuitry comprises a digital-to-analog converter which can be calibrated with calibration values held in the EEPROM.

11. (original) The integrated circuit of claim 10, further including a micro-controller arranged to cause the digital-to-analog converter to acquire its calibration values.

12. (original) The integrated circuit of claim 10, further including a micro-controller arranged to write to the EEPROM calibration values for the digital-to-analog converter.

13. (original) The integrated circuit of claim 1, wherein the EEPROM is divided into at least two separate memories which are selected from the group comprising bootstrap memory, program memory and data memory, and wherein the at least two memories are of the same construction.

14. (original) The integrated circuit of claim 1, further including a digital-to-analog converter selected from the group comprising a string digital to analog converter and a current source digital to analog converter; and an operational amplifier coupled to the digital to analog converter output.

15. (original) The integrated circuit of claim 1, further including a micro-controller and a serial port, the micro-controller arranged to download a user's program via the serial port and to write it into the EEPROM.

16. (original) The integrated circuit of claim 1, further including a device for generating voltages for programing the EEPROM and erasing the EEPROM.

17. (original) The integrated circuit of claim 16, wherein the device for generating the programming and erase voltages is a charge pump.

18. (cancelled)

19. (cancelled)

20. (cancelled)

21. (cancelled)

22. (cancelled)

23. (cancelled)

24. (cancelled)

25. (cancelled)

26. (original) A CMOS integrated circuit including analog and digital circuitry, said circuit having two polysilicon layers on a CMOS substrate, wherein said digital circuitry includes an EEPROM memory comprising a floating gate formed from a first one of the polysilicon layers

and a control gate formed from a second one of the polysilicon layers, and said analog circuit comprises a digital-to-analog converter which can be calibrated using calibration values stored in said EEPROM.

27. (original) The CMOS integrated circuit of claim 26, further including means for erasing the EEPROM by tunneling between polysilicon layers.

28. (original) The CMOS integrated circuit of claim 26 in which the digital-to-analog converter is a current source DAC having a calibratable array of current sources.